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Optimization of a Post Via Etch Wet Clean Process Using a Novel, Full-Wafer Inspection Technique for Non-Visual Defects

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Problem Statement

- Electrical test data for a 90nm fab process highlighted a yield loss issue for center of wafer die
- Traditional inspection techniques using optical and e-beam tools were unable to detect the issue
- In this paper, we present results on optimizing a post via wet clean process that eliminates the center of wafer die yield loss mechanism

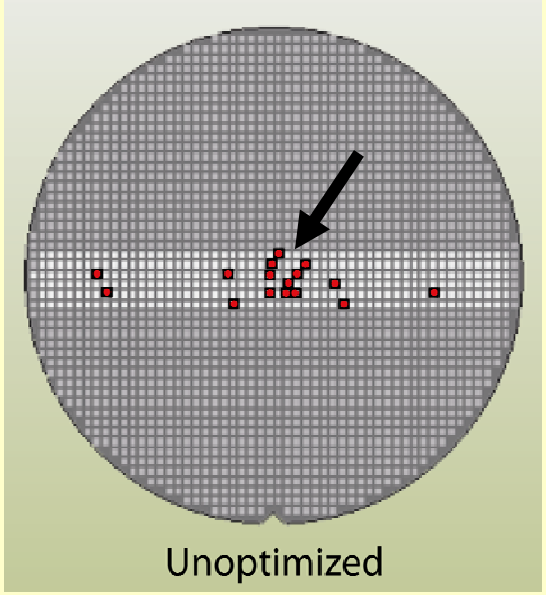


Figure 1

Bin maps from a 90nm fab highlight a yield loss mechanism impacting the center of wafer die

Non-Visual Defects (NVDs)

- "Defects that cause electrical failure, but do not leave behind a physical remnant that can be affordably detected with today's detection techniques, are called **non-visual defects**. As circuit designs become more complex, more circuit failures will be caused by defects that leave no detectable physical remnant"(1) based on the use of traditional defect inspection techniques.

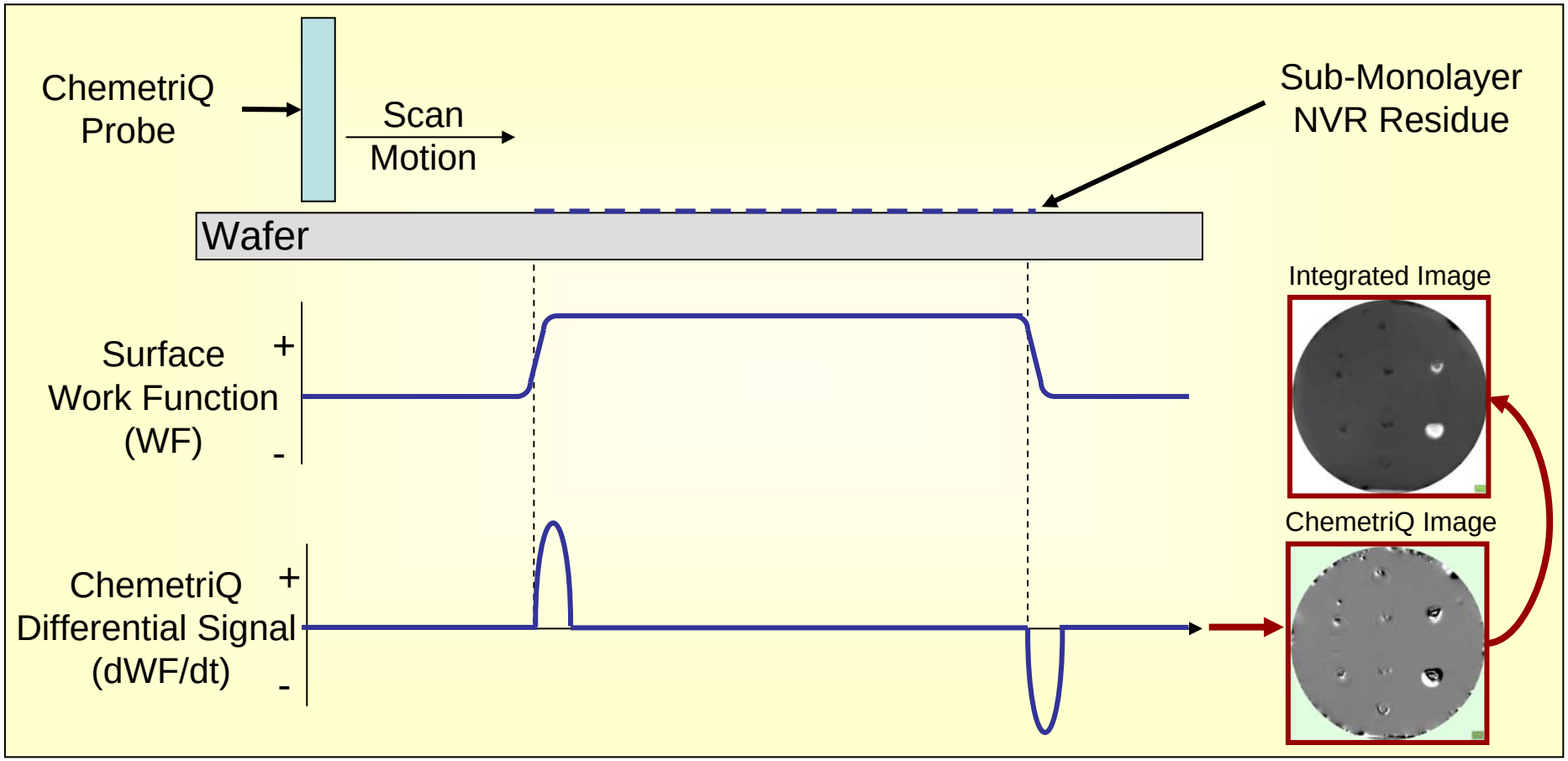
(1) The International Technology Roadmap for Semiconductors (ITRS) 2005 Edition, Yield Enhancement, page 18.

Non-Visual Defects (NVDs)

	Defect Examples	Inspection Techniques	Review and Classification Techniques
Physical Defects	• Particles • Scratches • Pits • Bridging	• Laser Scattering • Optical Imaging • E-Beam	• Optical Review • SEM/EDX
Non-Visual Defects	• Trace Metallics • Organics & Inorganics • Watermarks • Charging	**ChemetriQ® Inspection** (Scanning Differential Work Function)	• Analytical Tools • TXRF • TOF-SIMS • VPD/ICPMS

NVD Inspection with ChemetriQ

The ChemetriQ probe scans the wafer to detect changes in surface work function related to NVDs, and software creates a ChemetriQ Image



C.Yang, et al; MICRO Magazine V.25.1; Inspecting Wafers Using a Potential Difference Imaging Sensor Method, (2005)

Post Etch Residues

- After the via etch process, post etch residues are present on the sidewalls and floor of the via
- The challenge – how to remove the etch residues and ensure the removal of the cleaning chemistry
- It is critical that the rinsing step following the wet chemistry clean is highly efficient and effective

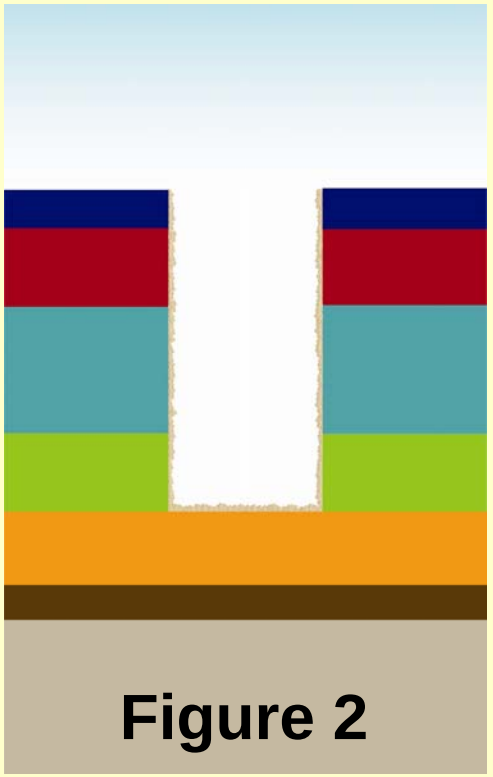


Figure 2

Via structure after etching, with etch residues on the sidewalls and floor of the via

Post Wet Clean Residues

- If the rinse in not highly efficient, then sub-monolayer residues and vapors may be present in the via
- Fab process engineers are driven by competing forces when trying to optimize the rinse process time
  - Reduce rinse times & DI usage
  - Efficient and effective rinsing
- The proper balance is a challenge

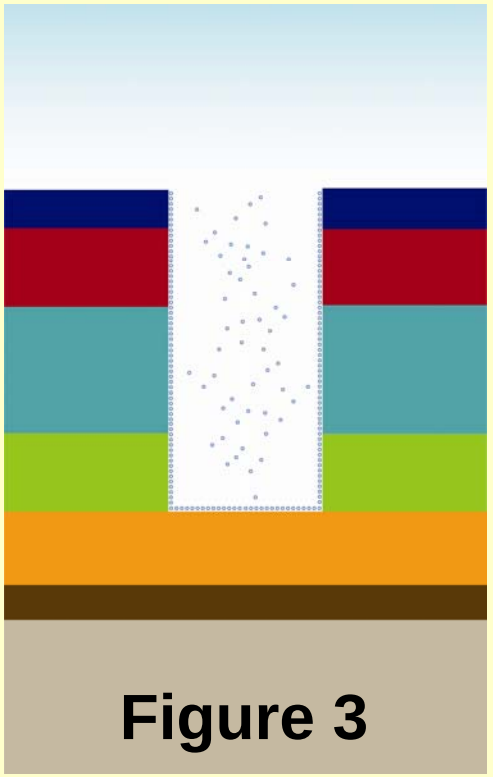


Figure 3

A post wet clean via showing a monolayer of residue and vapor that may be present in the via

Via Outgassing Phenomenon

- The sub-monolayer residues and vapors can diffuse from the via to create a surface residue
- This phenomenon is referred to as via outgassing, and can result in device degradation & yield loss
- The via outgassing residues are NVDs, and thus difficult to detect using traditional inspection tools

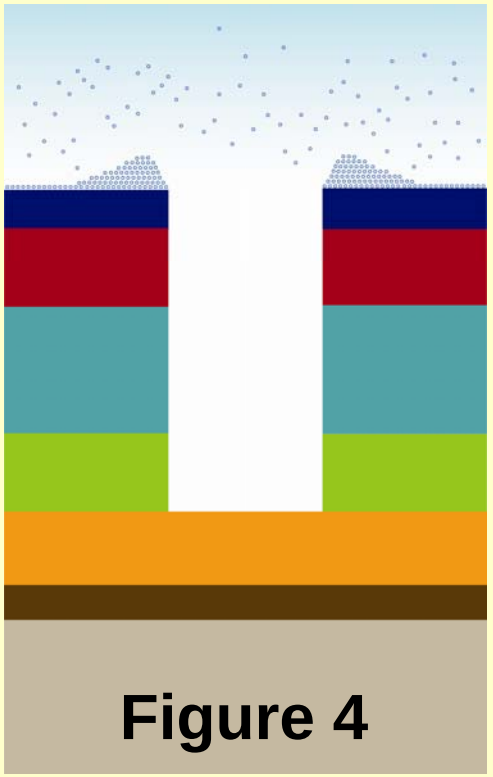


Figure 4

Scenario whereby post wet clean residues in the via outgas and deposit on the wafer surface

Experimental Design – Parameters

Test Wafers	130nm etched vias 2.5-to-1 aspect ratio
Wet Clean Process Flow	Wet Clean (using ATMI ST250) DI Water Rinse Spin Dry (using IPA/N_2 Process)
Experimental Split	(1) Stationary Rinse Nozzle 5mm off center (2) Sweep Rinse Nozzle translated across Wafer Center
NVD Inspection	(A) Immediately after Wet Clean Processing (B) After 24 hours of Storage to allow for Via Outgassing

Experimental Design – Notes

- Why use a Sweep Rinse Nozzle
  - Disrupt the boundary layer of liquid to introduce higher levels of turbulence in order to increase the turbulent diffusivity of liquid at the via surfaces
- NVD Inspection for Via Outgassing
  - Via outgassing was most evident after storage of the processed wafers in a cassette for 24 hours after the wet clean and DI rinse processing

Experimental Results – Stationary Nozzle

- Inspection results for the DI rinse using the stationary nozzle shows the presence of via outgassing
- The via outgassing signature as shown on the ChemetriQ Image is not detectable by traditional tools
- The location of the via outgassing signature matched the typical die loss pattern as shown in Figure 1

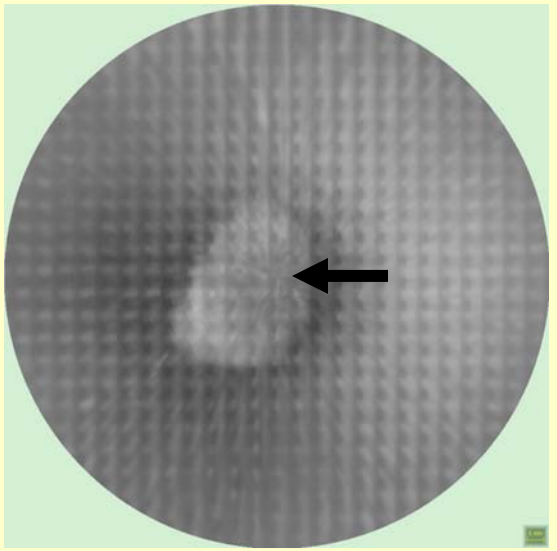


Figure 5

ChemetriQ data clearly showing the presence of a via outgassing event at the center of the wafer

Experimental Results – Sweep Nozzle

- Use of the sweep nozzle rinse process enabled higher efficiency for removal of the via residues
- Having the ability to detect the via outgassing NVDs enabled the fast optimization of the rinse process
- The ChemetriQ Image to the right shows that the via outgassing was eliminated with a sweep rinse

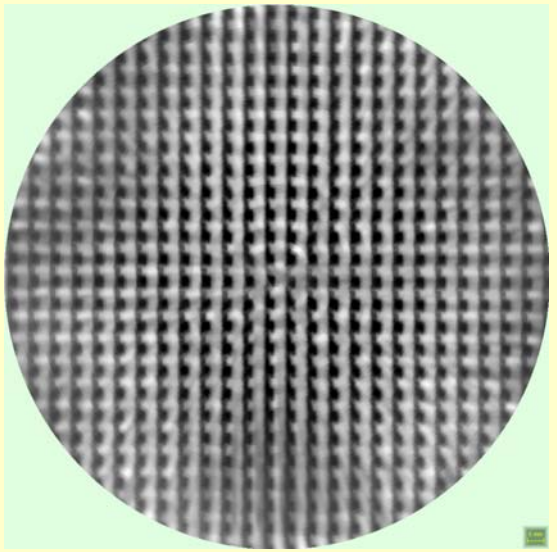


Figure 6

ChemetriQ data using the sweep nozzle rinse recipe, eliminating the via outgassing event

Verification in a 90nm Production Fab

- The optimized sweep nozzle rinse process was implemented in a fab running a 90nm via technology
- Yield results on product wafers matched expectations, eliminating the center of wafer yield loss
- These results validate that NVD inspection enables fast, efficient optimization of wet processes

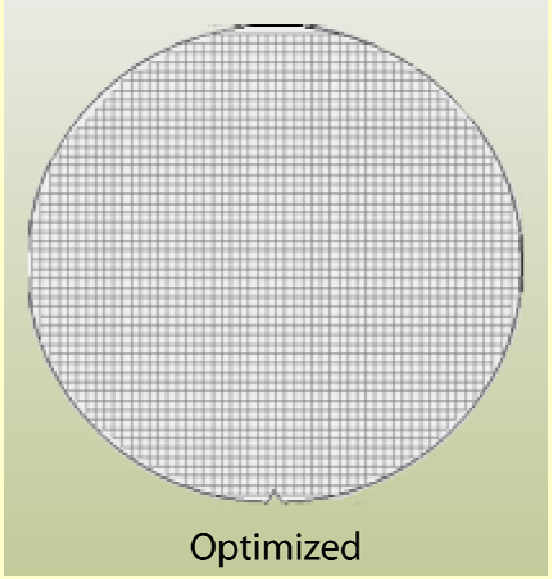
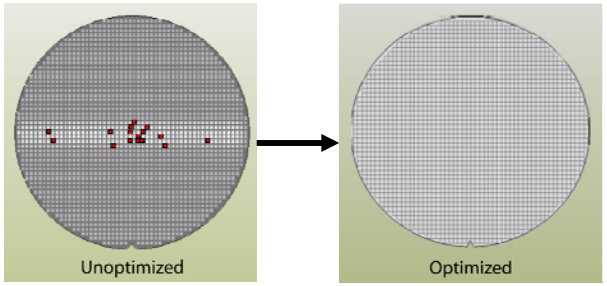


Figure 7

Bin map from a 90nm fab where the sweeping nozzle rinse improved center of wafer yields

Benefits Gained by 90nm Production Fab

Yield Enhancement	Elimination of Via Outgassing Resulted in Increased Yields	
Throughput Improvement	Total Rinse Time Reduced by 30% Using Sweep Nozzle Rinse	Platform Throughput Increase of 10 wph
Cost Reduction	Total Rinse Time Reduced by 30% Using Sweep Nozzle Rinse	Lower Costs Realized by Reduced DI Water Usage (~625 ml / wafer)

Summary Statement

- A post via etch wet clean process was optimized to eliminate via outgassing as an NVD yield issue
- The use of ChemetriQ Inspection for NVD detection enabled the development of the optimized process
- The optimized process utilized a sweeping nozzle rinse step on the Semitool single wafer clean tool
- Verification in a 90nm fab showed increased yields, higher tool throughputs and reduced DI water costs